PATENT
Attorney Docket No. 054216-5019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Ga Won LEE

Application No.: 10/028,972

Filed: December 28, 2001

For: METHOD OF FORMING INTER-DIELECTRIC LAYER IN SEMICONDUCTOR DEVICE

Confirmation No. 3736

Group Art Unit: 2812

Examiner: L. Gurley

Commissioner for Patents
Washington, DC 20231

Sir:

RESPONSE TO AN ELECTION REQUIREMENT

In an Election Requirement dated February 25, 2003 (Paper No. 6), the Examiner required election under 35 U.S.C. § 121 between Species I (pages 3-4 of the specification), Species II (page 4, second paragraph of the specification) or Species III (page 4, third paragraph of the specification). Applicant hereby elects Species II for examination and respectfully request formal examination of this application. It is respectfully submitted that at least claims 1-2 and 5-6 are readable thereon Species II.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,
MORGAN, LEWIS & BOCKIUS LLP

Dated: March 21, 2003

By: _____
Victoria D. Hao
Registration No. 47,630

Customer No.: 009629
MORGAN, LEWIS & BOCKIUS LLP
1111 Pennsylvania Avenue, N.W.
Washington, D.C. 20004
Telephone: 202.739.3000

PATENT
Attorney Docket No.: 054216-5019

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	)	
	)	
Ga Won LEE	)	
	)	
Application No.: 10/028,972	)	Group Art Unit: 2812
	)	
Filed: December 28, 2001	)	Examiner: Unassigned
	)	
For: METHOD OF FORMING INTER-DIELECTRIC LAYER IN SEMICONDUCTOR DEVICE	)	

Commissioner for Patents
Washington, D.C. 20231

Sir:

PRELIMINARY AMENDMENT

Prior to an examination on the merits, please amend the above-identified application as follows.

IN THE CLAIMS:

Please amend claims 1 – 8 as follows.

1. (Amended) A method of forming an interlayer dielectric film in a semiconductor device, the method comprising:

forming an insulating film spacer on a sidewall of a conductive layer pattern at a contact plug formation region; and

forming an interlayer dielectric film on an entire surface of the semiconductor device.

2. (Amended) The method according to claim 1, wherein said conductive layer pattern comprises one of a word line and a bit line.

3. (Amended) A method of forming an interlayer dielectric film in a semiconductor device, the method comprising: